

## **Summary**

A video chip designer, entrepreneur, and intellectual property business developer

## **Employment History**

**YAP IP**, Silicon Valley, California

**Founder and Leader**, 2008-2010

- Planned the architecture of a multicore superscalar RISC processor with SIMD extensions, designed to provide ARM Cortex A9 performance at lower cost without infringing patents
- Wrote the multiplier, ALU, instruction fetch, pipeline, and load/store logic core in Verilog
- Lead a team working on coherent cache controllers and an FPGA prototype
- Developed and pitched the business plan to Foundation Capital, NEA, and Tallwood VCs
- Created web site, trade show booth, brochures, and promotional giveaways

**Tensilica**, Santa Clara, California

**Mobile Multimedia Marketing Manager**, 2007-2008

- Managed marketing of Tensilica's video solutions, including the VDO video DSP product line
- Discussed requirements with all video customers and prospects worldwide, including frequent travel to China, Taiwan, and Korea and meetings with top executives
- Gathered data and kept a spreadsheet matrix quantifying development projects versus prospective deals, for executive comparison to engineering costs
- Performed SWOT analysis on competitors while seeking opportunities for collaboration
- Helped to close 5 IP licensing deals and was technical liaison during customer chip designs
- Interpreted specs between Indian software developers and Chinese customers
- Wrote articles and white papers and gave presentations at conferences and a webcast

**ARC International**, San Jose, California

**Director of Solutions Architecture**, 2006-2007

- Discussed requirements with each video customer and prospect worldwide, including frequent travel to China, Taiwan, Korea, and Japan and meetings with top executives
- Helped to close 10 IP licensing deals totaling as much as \$40M in revenue
- Worked from Silicon Valley with a UK engineering team
- Performed product analysis, identifying a fundamental design flaw
- Wrote product documentation, articles, white papers, and gave presentations at conferences

**Ultra Data**, Waltham, MA, USA (acquired in 2005 by **Micronas**, Freiburg, Germany)

**Principal Design Engineer**, 2003-2006

- Co-founded the company, which developed the first programmable processor architecture capable of 1080p HD decode of H.264 (AVC) and other video standards
- Performed architecture analysis and essentially all of the Verilog design of a two-issue VLIW DSP core, a simple RISC core, and a 5 core multiprocessor with RAMs, FIFOs, and DMA
- Iteratively negotiated ISA changes with software developers to trade off architectural performance with clock speed
- Applied for two patents
- Built an FPGA prototype of the processor as Altera's first external Nios II customer
- Worked remotely with a multinational engineering team
- Wrote papers, gave talks, evangelized our technology, and developed collateral
- Negotiated sales deals with top tier semiconductor and consumer electronics companies
- Negotiated and closed the acquisition of the company, yielding a 15x ROI for investors

**Lexra**, Waltham, MA

**Design Engineer**, 1999-2002

- Designed the multiply-accumulator, a key part of DSP extensions to the MIPS32 ISA for which Lexra was known
- Designed, documented, and supported an FPGA-based devboard, including peripheral IP
- Wrote block and system level directed verification tests in Verilog, Perl, and assembly

**Teradyne**, Boston, MA

**Test Development Engineer**, 1998-1999

- Developed manufacturing test processes for mixed-signal testers for disk drive chips

**Rampage Systems**, Waltham, MA

**Engineering Intern**, 1995-1997

- Automated mfg test, board debug, and failure analysis for PCI screener and FFP boards
- Designed FPGA-controlled PC peripheral hardware platform to perform testing
- Wrote a LAN network bandwidth test program

## **Project Work**

**EE Times**, 2010

- Freelance reporter

**Arasan Chip Systems**, 2009

- Performed prior art search and patent application drafting

**Poseidon Design Systems**, 2006

- Developed a specification for a size and power efficient H.264 I-frame decoder IP core

**VideoBits.org**, 2005-2008

- Published a web-based tutorial on principles of digital video
- Maintained a directory of hundreds of video technology companies and products
- Maintained contact with industry leaders, connecting people with opportunities
- Built a thorough collection of video coding test sequences

**Omnilala**, 2005-present

- Advise CEO on SoC selection, design specs, and strategy for networked media players, servers, and other home entertainment multimedia products

**On2 Technologies**, 2004

- Wrote an opinion and testified as an expert witness in a codec license fee case

**Altera**, 2004

- Developed an IP core design specification with an eye towards testability and maintainability

## **Education**

**Cornell University**, Ithaca, NY

**Bachelor of Science in Electrical Engineering**, 1994-1998

- Architected, designed, and prototyped Methos 16-bit RISC processor core
- Three years as teaching assistant for a freshman class on compact disc technology

## **Honors**

- Westinghouse Science Talent Search 1994 semifinalist and Massachusetts State Science Fair first place winner for project *Identifying Bacteria by Their Reflectance Spectra*
- Embedded Processor Forum 2004 presentation *The Ultra Data UD3000: A Next Generation Video Processor Core*

- 2006 Picture Coding Symposium (Beijing) invited paper *Architecture Considerations for Multi-Format Programmable Video Processors* (published in IEEE Journal of Signal Processing Systems for Signal, Image, and Video Technology)
- Invited guest lecturer on digital video technology at Cornell University

## **Industry Group Participation**

**Synopsys Users Group (SNUG) Technical Committee**, 2007-present

- Review papers as a generalist

**Society of Motion Picture and Television Engineers (SMPTE)**, 2005-present

- Observe video technology developments

**DesignCon Technical Program Committee**, 2005-2008

- Reviewed chip design papers

**MPEG Industry Forum (MPEGIF)**, 2006-2007

- Represented ARC International

## **Selected Publications**

- EE Times article *Processor architecture not a factor for low-power mobile systems*
- Tensilica white paper *A Designer's Guide to HD Video Pre- and Post-Processing*
- ARC white paper *A Brief History of Video Coding*
- GSPx 2006 paper *System Design Tricks for Lower-Power Video Processing*
- IEEE Journal of Signal Processing Systems for Signal, Image, and Video Technology *Architecture Considerations for Multi-Format Programmable Video Processors*
- GSPx 2004 paper *What Choices Make a Killer Video Processor Architecture*
- Embedded Processor Forum *The Ultra Data UD3000: A Next Generation Video Processor*

## **Skills**

- Basic level Mandarin Chinese, steadily improving
- Self taught SystemVerilog
- Good understanding of H.264 AVC, MPEG-2, VP6, WMV9 (VC-1), Real codecs
- C and assembly language programming, Perl and Bash shell scripting, HTML, XML
- Various degrees of EDA tool experience including Synopsys VCS, Design Compiler, IC Compiler, Prime Time, and Synplicity Synplify, Cadence NC-Verilog XL, and RTL Compiler, Mentor ModelSim, Altera Quartus II, Xilinx ISE, and Matlab
- Microsoft Word, Excel, and PowerPoint and Adobe Photoshop and Illustrator

## **Interests**

- Wikipedia
- Sailing
- Human languages
- Low-cost consumer electronic gadgets

## **Epilog**

I have broad experience. I learn quickly and have a record of producing results. I am quantitative, rigorous, and bring a diverse perspective to any group.